

# Paul Nieves

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## EDUCATION

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<b>Rensselaer Polytechnic Institute</b> , Troy, NY	<b>Expected Graduation:</b> May 2025
M.S. Electrical Engineering (Concentration: Computer Systems Design)	<b>GPA:</b> 3.33
<b>Rensselaer Polytechnic Institute</b> , Troy, NY	<b>Graduation:</b> May 2024
B.S. Electrical and Computer Systems Engineering Dual	<b>GPA:</b> 3.48

## EXPERIENCE

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<b>Green Action Studio</b> Schenectady, NY	<b>Sep 2022 – Dec 2022</b>
Embedded Hardware Engineer	
<ul style="list-style-type: none"><li>Engineered PCB modules for an electric vehicle charger and designed a UL-approved ground fault detection circuit.</li><li>Optimized ARM-based microcontroller firmware and assembled EV chargers from schematics</li></ul>	
<b>Claro Puerto Rico</b> Guaynabo, Puerto Rico	<b>May 2024 – Aug 2024</b>
Network Technician	
<ul style="list-style-type: none"><li>Maintained demarcation points for residential and commercial clients (Demarcation points: Tmarc, ASR 9k/920, Cisco 3000)</li><li>Diagnosed and resolved signal loss and connectivity issues for fiber optics, copper, and coaxial networks</li></ul>	

## PROJECTS

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<b>Pipelined RISC-V Processor Implementation</b> Troy, NY	
<i>ECSE 4770 - Computer Hardware Design</i>	
<ul style="list-style-type: none"><li>Designed a 5-stage pipelined processor supporting key RISC-V instructions with hazard detection</li><li>Extended datapath and control logic to implement Load Upper Immediate (lui)</li><li>Verified functionality through SystemVerilog testbench, RTL schematics, and waveform analysis</li></ul>	
<b>Static CMOS Logic Design &amp; Layout for VLSI (65 nm)</b> Troy, NY	
<i>ECSE 4220 – VLSI Design</i>	
<ul style="list-style-type: none"><li>Optimized a CMOS circuit using Karnaugh maps, minimizing transistor count for efficiency</li><li>Developed a compact, DRC-compliant layout with minimal interconnects</li><li>Verified through Layout vs. Schematic (LVS) and performed parasitic extraction (PEX)</li></ul>	
<b>Deep Q-Learning for CartPole Control Problem</b> Troy, NY	
<i>ECSE 6965 – Reinforcement Learning</i>	
<ul style="list-style-type: none"><li>Implemented a Deep Q-Network (DQN) to balance a pole using reinforcement learning</li><li>Designed a neural network from scratch with experience replay and a target network for stable learning</li><li>Tuned hyperparameters, achieving an average reward of 200 over 100 episodes</li></ul>	
<b>Modular Synth</b> Troy, NY	
<i>ECSE 6980 - Masters Project</i>	
<ul style="list-style-type: none"><li>Designed PCBs for VCO, VCA, MIDI-to-CV, ADSR, and a <math>\pm 15V/\pm 20V</math> DC power supply for a modular synthesizer</li><li>Programmed firmware for Arduino Nano (ARM) to interface with 16-bit DACs through SPI for 1mV precision analog note</li></ul>	

## RESEARCH

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<b>LESA Florescence Tool Research</b> Troy, NY	<b>Sep 2023 – Dec 2023</b>
Software Engineer/Embedded Hardware Engineer	
<ul style="list-style-type: none"><li>Built, integrated, and tested Fluorescence tool hardware for plant health analysis</li><li>Debugged and enhanced Lock-in Amplifier Circuit by adding filters to better detect fluorescence wavelength from plants</li></ul>	
<b>Photonics GUI Research</b> Troy, NY	<b>Sep 2023 – Dec 2023</b>
Software Engineer/Embedded Hardware Engineer	
<ul style="list-style-type: none"><li>Automated Tektronix oscilloscope, multimeter, and function generator with Python via GPIB (py-visa)</li><li>Developed a GUI for streamlined test execution and result storage. (Integrated cloud saving into GUI)</li></ul>	

## SKILLS

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<b>Programming:</b> C++, C, Python, Java, SystemVerilog, MIPS, VHDL
<b>Hardware Design:</b> PCB Design (Altium, KiCAD, EAGLE), FPGA Design, VLSI Layout, CAD
<b>Software &amp; Tools:</b> MATLAB, Quartus Prime, Vivado, ModelSim, Cadence, LTSpice, LabVIEW, Fusion 360, Arduino IDE
<b>Languages:</b> Fluent in English & Spanish
<b>Coursework:</b> Reinforcement Learning, Advanced VLSI Design, Advanced Computer Hardware Design, Embedded Control, Digital Signal Processing, Microelectronics Technology, Electrical Energy Systems, Mechatronics, Linear Algebra, Multivariable Calculus